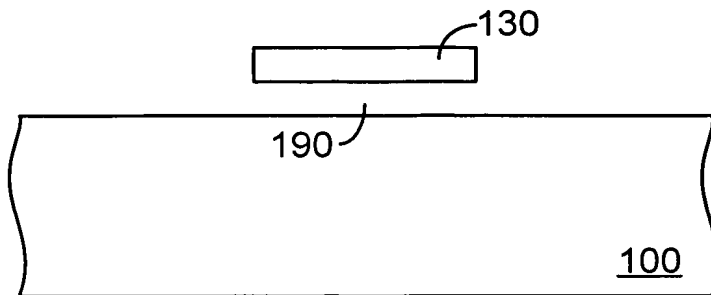


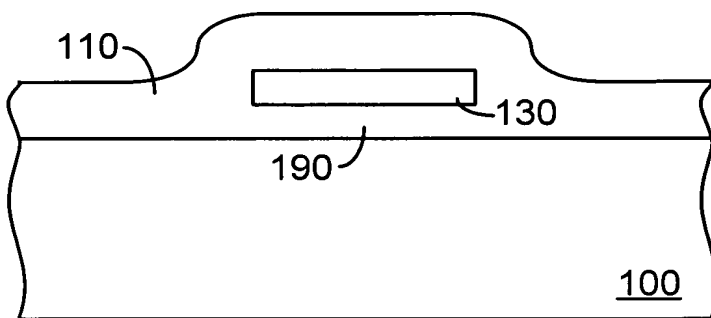


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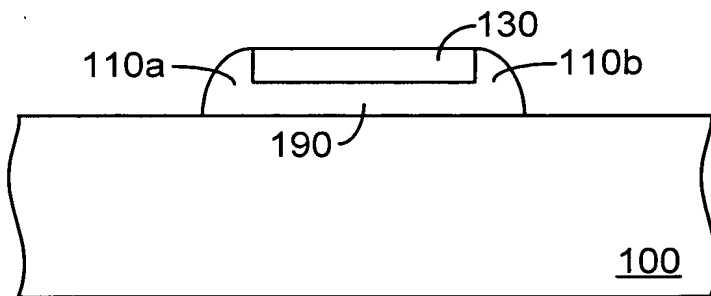
**Fig. 1a**



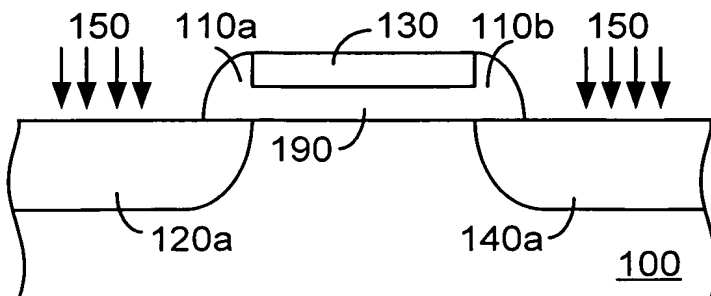
**Fig. 1b**



**Fig. 1c**



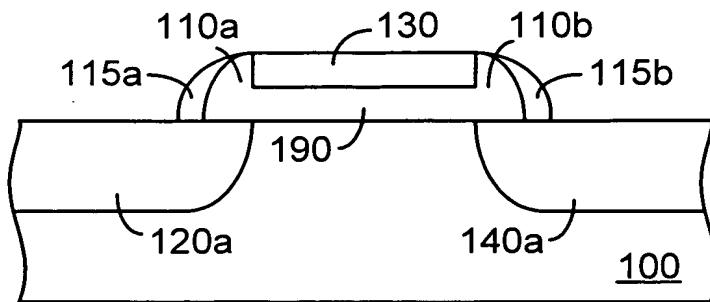
**Fig. 1d**



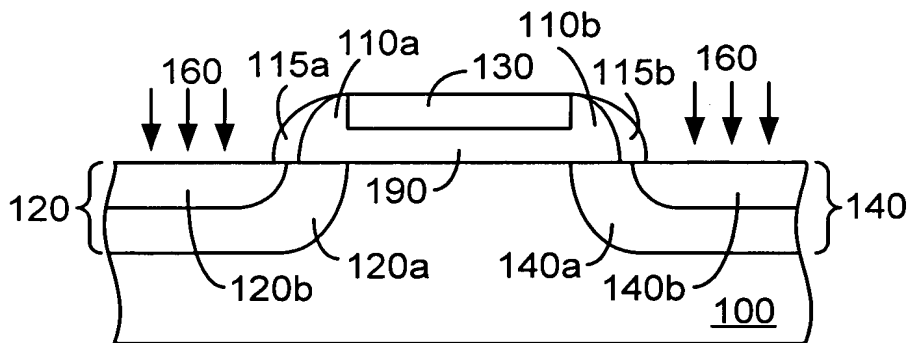


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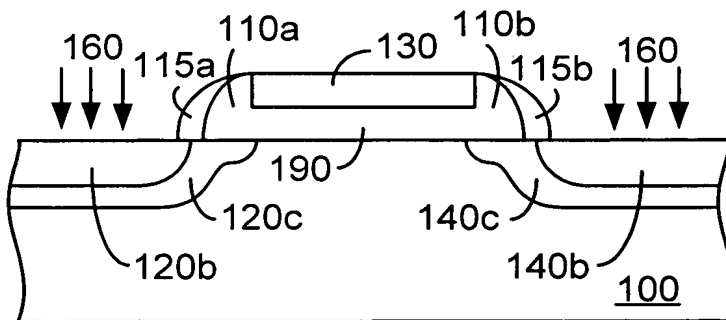
**Fig. 1e**



**Fig. 1f**

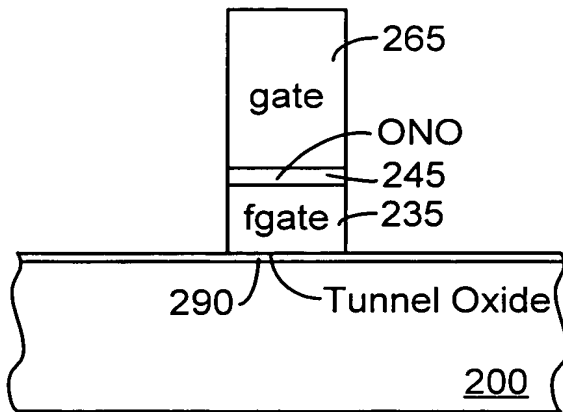


**Fig. 1g**

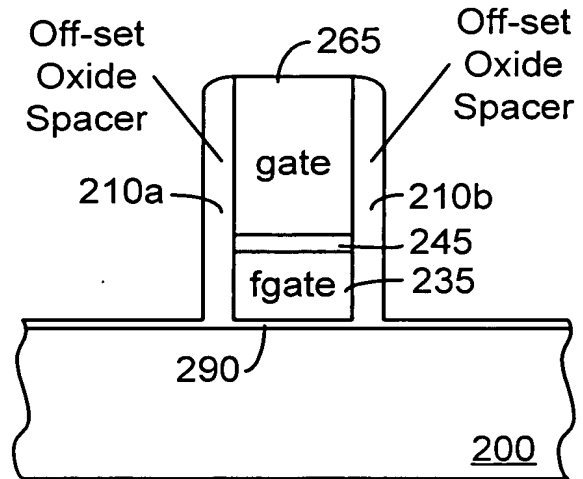




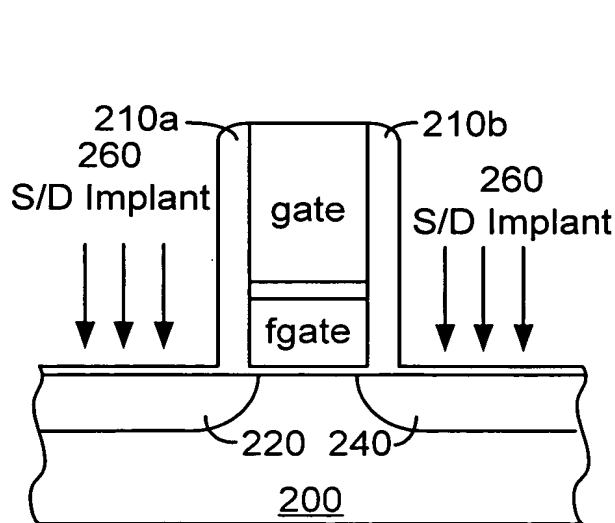
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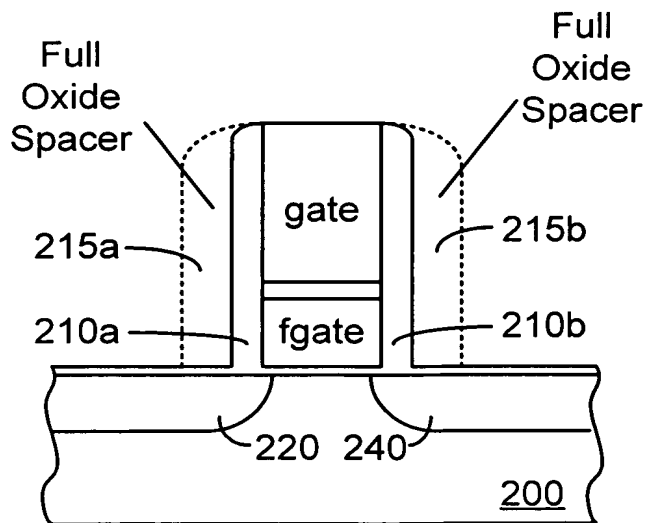
**Fig. 2a**



**Fig. 2b**



**Fig. 2c**



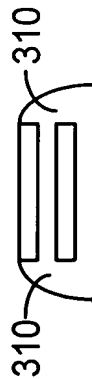
**Fig. 2d**

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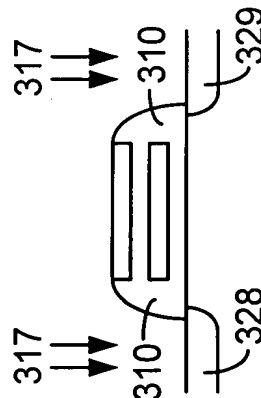
Array Cell



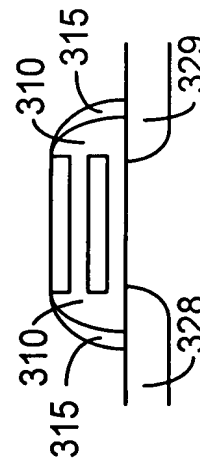
**Fig. 3a**



**Fig. 3b**

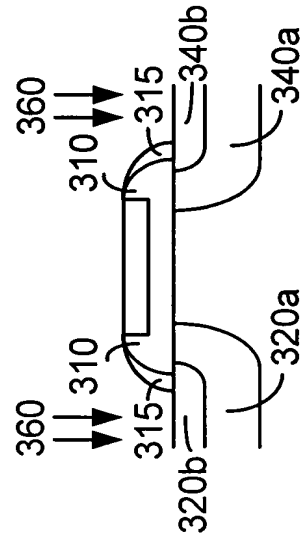
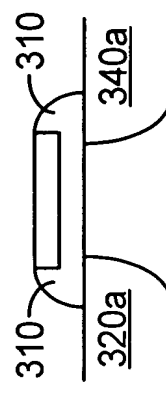
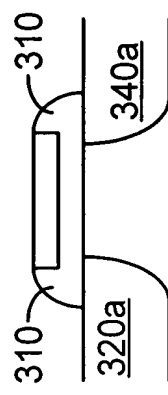
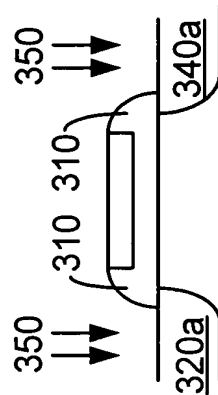


**Fig. 3c**

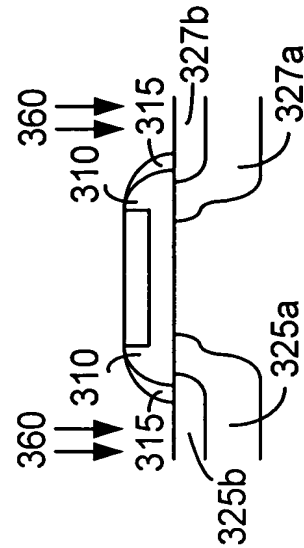
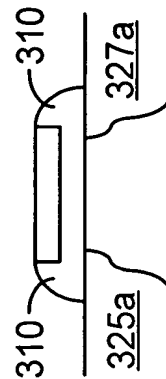
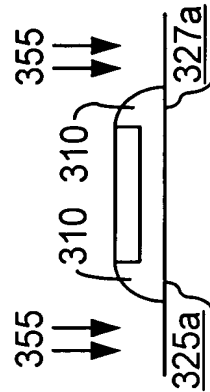


**Fig. 3d**

Periphery DDD  
HV transistor



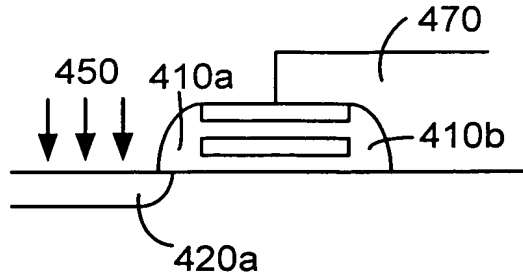
Periphery LDD  
LV transistor



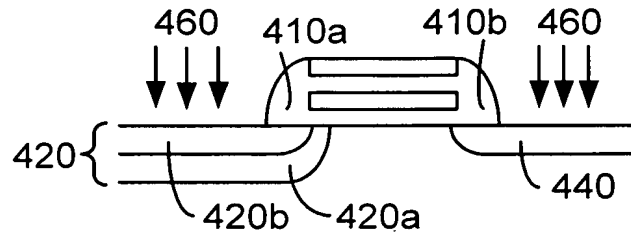


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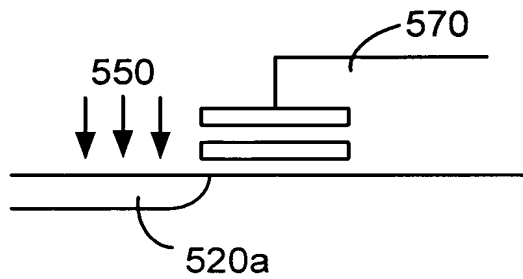
**Fig. 4a**



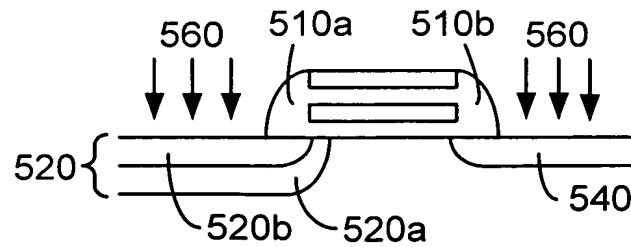
**Fig. 4b**

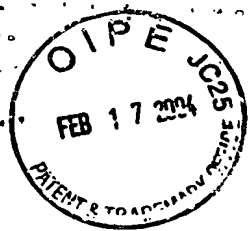


**Fig. 5a**

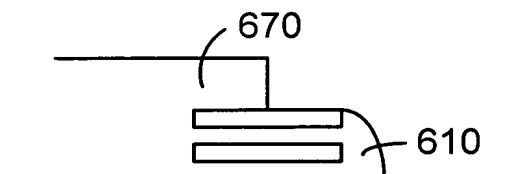


**Fig. 5b**





**Fig. 6**



**Fig. 7**

